KAI-29052

6576 (H) x 4384 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Figure 1. KAI−29052 CCD Image Sensor

Description

The KAI−29052 Image Sensor is a 29 Megapixel CCD in a 35 mm optical format that provides increased Quantum Efficiency (particularly for NIR wavelengths) compared to members of the standard 5.5 μm family.

The sensor shares the same broad dynamic range, excellent imaging performance, and flexible readout architecture as other members of the 5.5 μm pixel family. However, QE at 820 nm has been approximately doubled compared to existing devices, enabling enhanced sensitivity without a corresponding decrease in the Modulation Transfer Function (MTF) of the device.

The sensor is available with the Sparse Color Filter Pattern, which provides a 2× improvement in light sensitivity compared to a standard color Bayer part.

The KAI−29052 is drop-in compatible with the KAI−29050 Image Sensor, simplifying adoption by camera manufacturers currently working with the KAI−29050.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	6644 (H) × 4452 (V)
Number of Effective Pixels	6600 (H) × 4408 (V)
Number of Active Pixels	6576 (H) × 4384 (V)
Pixel Size	5.5 μm (H) × 5.5 μm (V)
Active Image Size	36.17 mm (H) × 24.11 mm (V) 43.47 mm (diag.), 35 mm Optical Format
Aspect Ratio	3:2
Number of Outputs	1, 2, or 4
Charge Capacity	20,000 electrons
Output Sensitivity	35 μV/e−
Quantum Efficiency Pan (−AXA, −QXA, −PXA) R, G, B (−FXA, −QXA)	 43%, 12%, 5% (540, 850, 920 nm) 39%, 40%, 37% (620, 540, 480 nm)
Read Noise (f = 40 MHz)	10 electrons rms
Dark Current Photodiode VCCD	 7 electrons/s 140 electrons/s
Dark Current Doubling Temp. Photodiode VCCD	 7°C 9°C
Dynamic Range	66 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 300 X
Smear	Estimated −100 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rates Quad Output Dual Output Single Output	 4 fps 2 fps 1 fps
Package	72 pin PGA
Cover Glass	AR Coated, 2 Sides

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

Features

- Increased QE, with 2× Improvement at 820 nm
- Bayer Color Pattern, Sparse Color Pattern, and Monochrome Configurations
- Progressive Scan Readout
- Flexible Readout Architecture
- High Frame Rate
- Low Noise Architecture
- Excellent Smear Performance
- Package Pin Reserved for Device Identification

Applications

- Industrial Imaging and Inspection
- Medical Imaging
- Security and Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAI−29052−AXA−JD−B1	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−29052−AXA Serial Number
KAI−29052−AXA−JD−B2	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1	
KAI−29052−AXA−JD−AE	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−29052−FXA−JD−B1	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−29052−FXA Serial Number
KAI−29052−FXA−JD−B2	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−29052−FXA−JD−AE	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−29050−QXA−JD−B1	Gen2 Color (Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−29052−QXA Serial Number
KAI−29050−QXA−JD−AE	Gen2 Color (Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	

Table 3. EVALUATION SUPPORT

Part Number	Description
G2−FPGA−BD−14−40−A−GEVK	FPGA Board for IT−CCD Evaluation Hardware
KAI−72PIN−HEAD−BD−A−GEVB	72 Pin Imager Board for IT−CCD Evaluation Hardware
LENS−MOUNT−KIT−C−GEVK	Lens Mount Kit for IT−CCD Evaluation Hardware

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

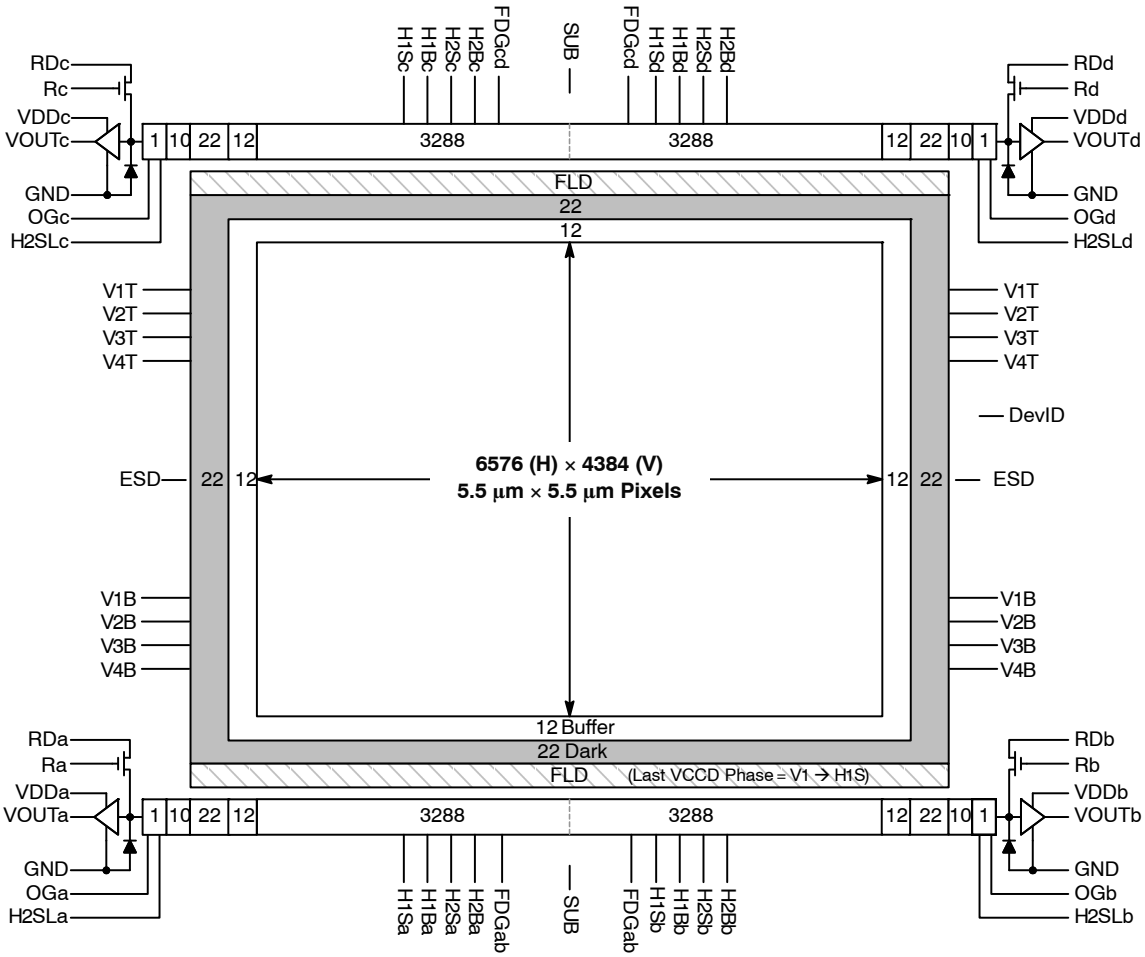


Figure 2. Block Diagram

Dark Reference Pixels

There are 22 dark reference rows at the top and 22 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 22 dark columns on the left or right side of the image sensor as a dark reference. Under normal circumstances use only the center 20 columns of the 22 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level. In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

12 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo-site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Bayer Color Filter Pattern

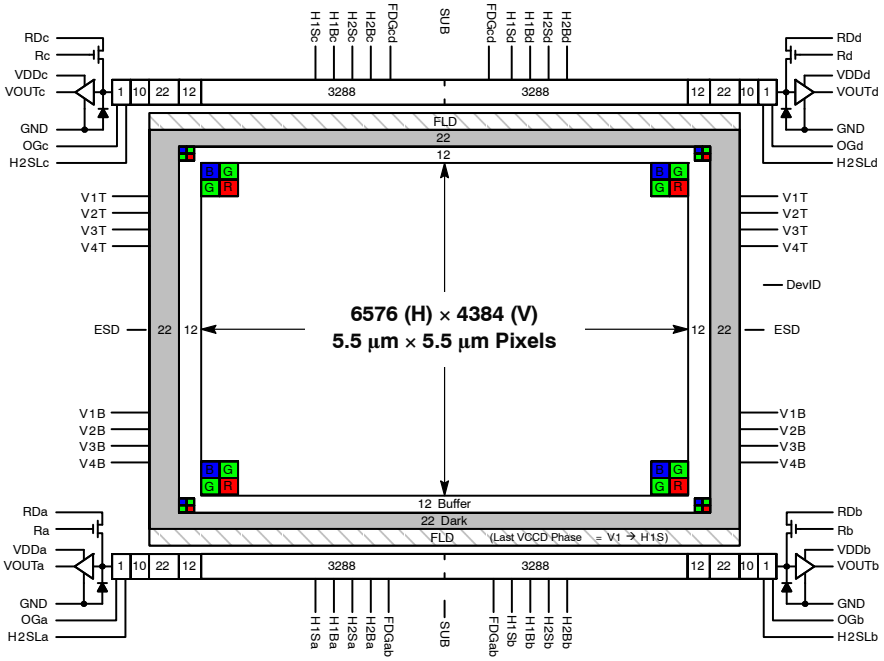


Figure 3. Bayer Color Filter Pattern

Sparse Color Filter Pattern

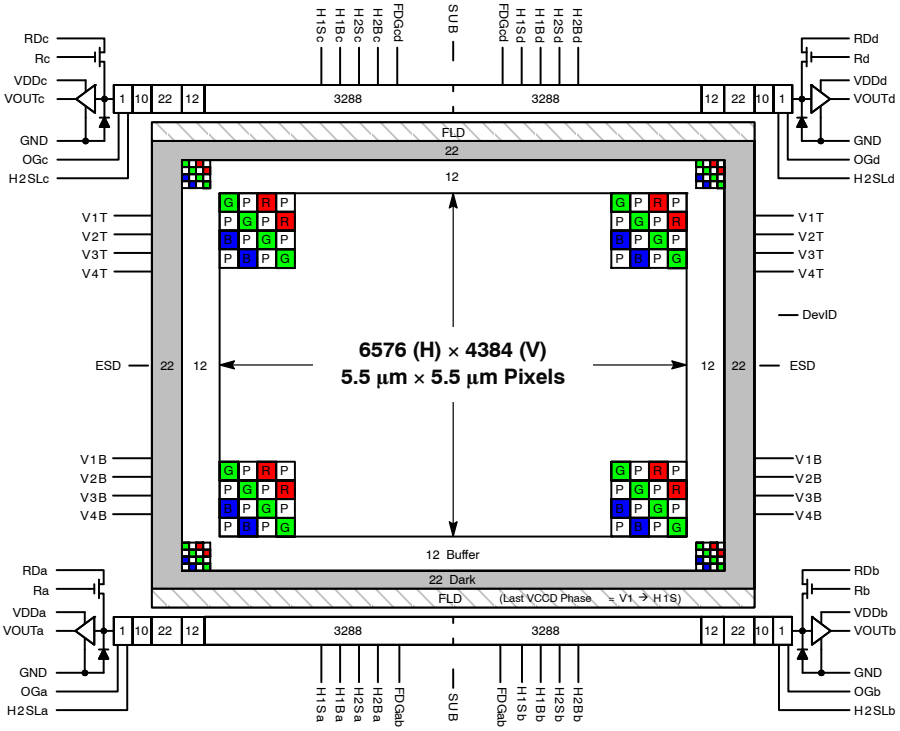


Figure 4. Sparse Color Filter Pattern

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

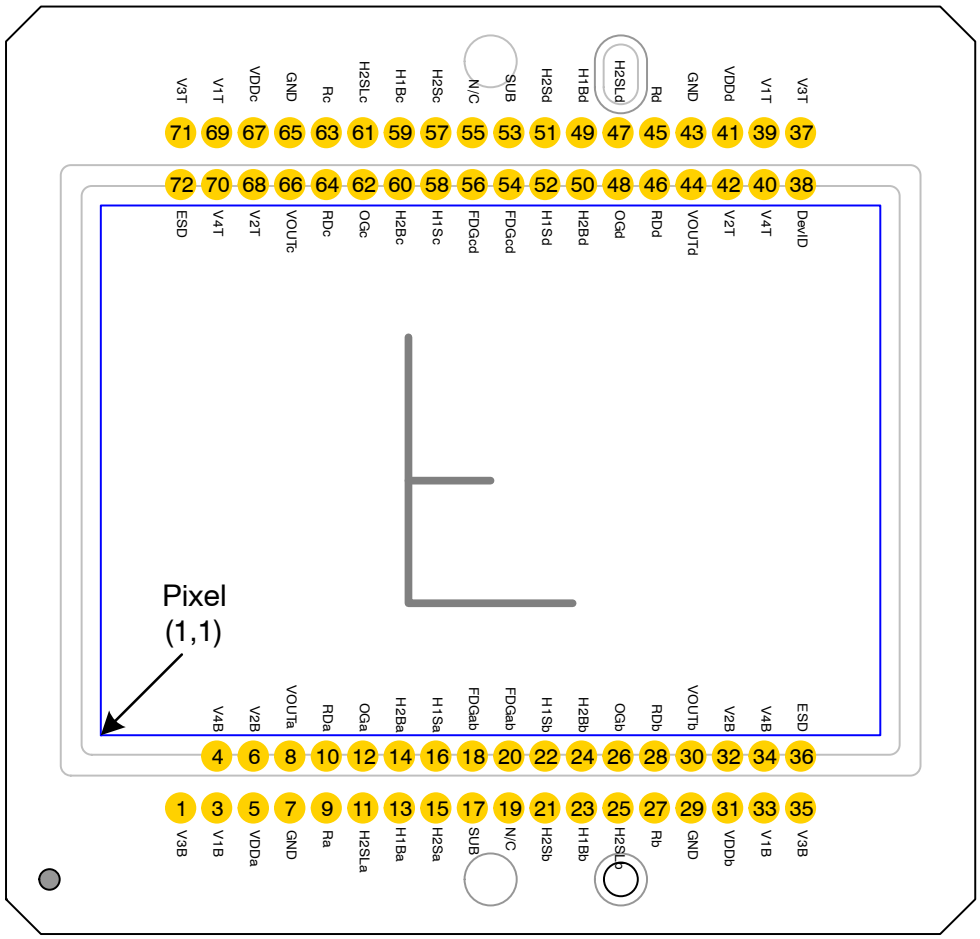


Figure 5. Package Pin Description (Top View)

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Quadrant a
10	RDa	Reset Drain, Quadrant a
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	SUB	Substrate
18	FDGab	Fast Line Dump Gate, Bottom
19	N/C	No Connect
20	FDGab	Fast Line Dump Gate, Bottom
21	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
22	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
23	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
24	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
25	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
26	OGb	Output Gate, Quadrant b
27	Rb	Reset Gate, Quadrant b
28	RDb	Reset Drain, Quadrant b
29	GND	Ground
30	VOUTb	Video Output, Quadrant b
31	VDDb	Output Amplifier Supply, Quadrant b
32	V2B	Vertical CCD Clock, Phase 2, Bottom
33	V1B	Vertical CCD Clock, Phase 1, Bottom
34	V4B	Vertical CCD Clock, Phase 4, Bottom
35	V3B	Vertical CCD Clock, Phase 3, Bottom
36	ESD	ESD Protection Disable

Pin	Name	Description
72	ESD	ESD Protection Disable
71	V3T	Vertical CCD Clock, Phase 3, Top
70	V4T	Vertical CCD Clock, Phase 4, Top
69	V1T	Vertical CCD Clock, Phase 1, Top
68	V2T	Vertical CCD Clock, Phase 2, Top
67	VDDc	Output Amplifier Supply, Quadrant c
66	VOUTc	Video Output, Quadrant c
65	GND	Ground
64	RDc	Reset Drain, Quadrant c
63	Rc	Reset Gate, Quadrant c
62	OGc	Output Gate, Quadrant c
61	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
60	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
59	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
58	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
57	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
56	FDGcd	Fast Line Dump Gate, Top
55	N/C	No Connect
54	FDGcd	Fast Line Dump Gate, Top
53	SUB	Substrate
52	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
51	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
50	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
49	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
48	OGd	Output Gate, Quadrant b
47	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
46	RDd	Reset Drain, Quadrant d
45	Rd	Reset Gate, Quadrant d
44	VOUTd	Video Output, Quadrant d
43	GND	Ground
42	V2T	Vertical CCD Clock, Phase 2, Top
41	VDDd	Output Amplifier Supply, Quadrant d
40	V4T	Vertical CCD Clock, Phase 4, Top
39	V1T	Vertical CCD Clock, Phase 1, Top
38	DevID	Device Identification
37	V3T	Vertical CCD Clock, Phase 3, Top

1. Like named pins are internally connected and should have a common drive signal.
2. N/C pins (19, 55) should be left floating.

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATION CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition
Light Source (Note 1)	Continuous Red, Green and Blue LED Illumination
Operation	Nominal Operating Voltages and Timing

1. For monochrome sensor, only green LED used.

Table 6. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Dark Field Global Non-uniformity	DSNU	–	–	5	mVpp	Die	27, 40
Bright Field Global Non-uniformity (Note 1)		–	2	5	%rms	Die	27, 40
Bright Field Global Peak to Peak Non-uniformity (Note 1)	PRNU	–	10	30	%pp	Die	27, 40
Maximum Photo-response Non-linearity (Note 2)	NL	–	2	–	%	Design	
Maximum Gain Difference Between Outputs (Note 2)	ΔG	–	10	–	%	Design	
Maximum Signal Error due to Non-linearity Differences (Note 2)	ΔNL	–	1	–	%	Design	
Horizontal CCD Charge Capacity	H_{Ne}	–	50	–	ke^-	Design	
Vertical CCD Charge Capacity	V_{Ne}	–	40	–	ke^-	Design	
Photodiode Charge Capacity (Note 3)	P_{Ne}	–	20	–	ke^-	Die	27, 40
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	–		Die	
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	–		Die	
Photodiode Dark Current	I_{PD}	–	7	70	e/p/s	Die	40
Vertical CCD Dark Current	I_{VD}	–	140	400	e/p/s	Die	40
Image Lag	Lag	–	–	10	e^-	Design	
Anti-blooming Factor	X_{AB}	300	–	–		Design	
Vertical Smear	Smr	–	−100	–	dB	Design	
Read Noise (Note 4)	n_{e-T}	–	10	–	e^-rms	Design	
Dynamic Range (Notes 4, 5)	DR	–	66	–	dB	Design	
Output Amplifier DC Offset	V_{ODC}	–	9.4	–	V	Die	27, 40
Output Amplifier Bandwidth (Note 6)	f_{-3db}	–	250	–	MHz	Die	
Output Amplifier Impedance	R_{OUT}	–	127	–	Ω	Die	27, 40
Output Amplifier Sensitivity	ΔV/ΔN	–	35	–	$\mu V/e^-$	Design	

Table 6. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
KAI−29052−AXA AND KAI−29052−QXA CONFIGURATIONS							
Peak Quantum Efficiency	QE_{MAX}	−	43	−	%	Design	
Peak Quantum Efficiency Wavelength	λ_{QE}	−	540	−	nm	Design	
Quantum Efficiency (850 nm)	QE_{MAX}	−	12	−	nm	Design	
Peak Quantum Efficiency (920 nm)	QE_{MAX}	−	5	−	nm	Design	
KAI−29052−FBA AND KAI−29052−QBA GEN2 COLOR CONFIGURATIONS							
Peak Quantum Efficiency Blue Green Red	QE_{MAX}	 − − −	 37 40 39	 − − −	%	Design	
Peak Quantum Efficiency Wavelength Blue Green Red	λ_{QE}	 − − −	 480 540 620	 − − −	nm	Design	

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is 700 mV.
4. At 40 MHz.
5. Uses 20 LOG (P_{Ne} / n_{e-T}).
6. Assumes 5 pF load.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

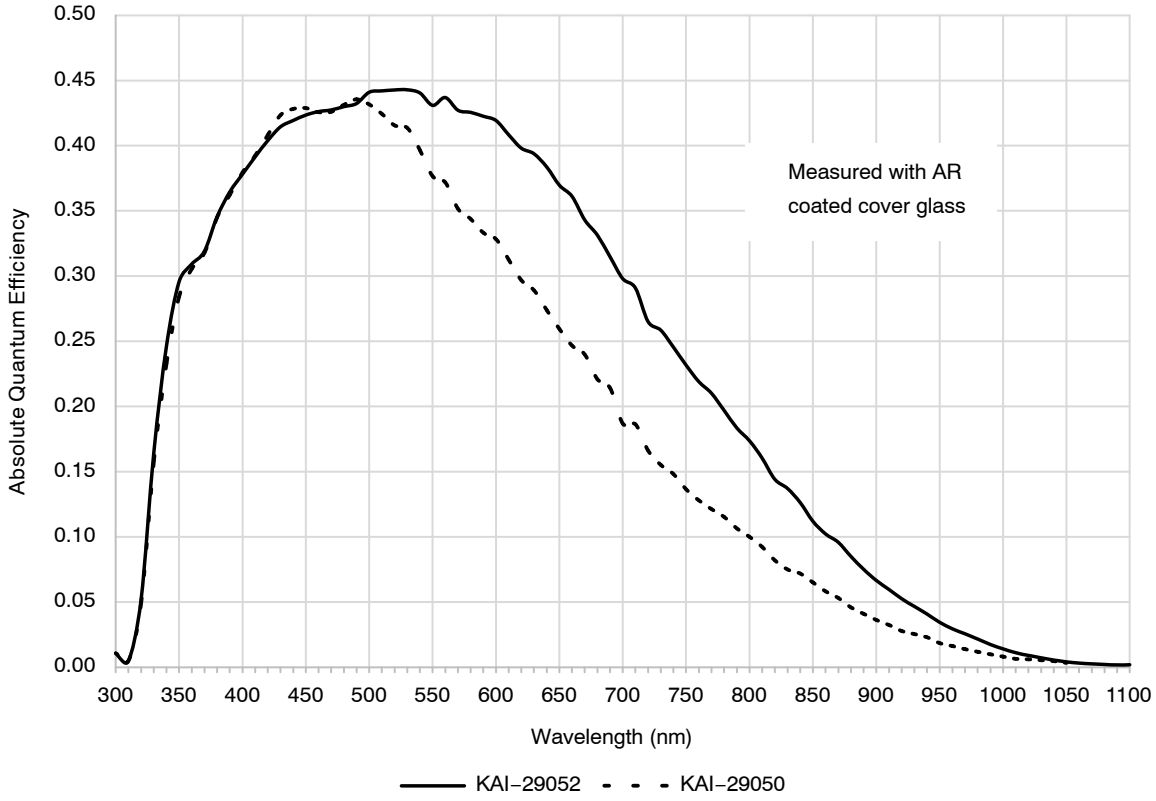


Figure 6. Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

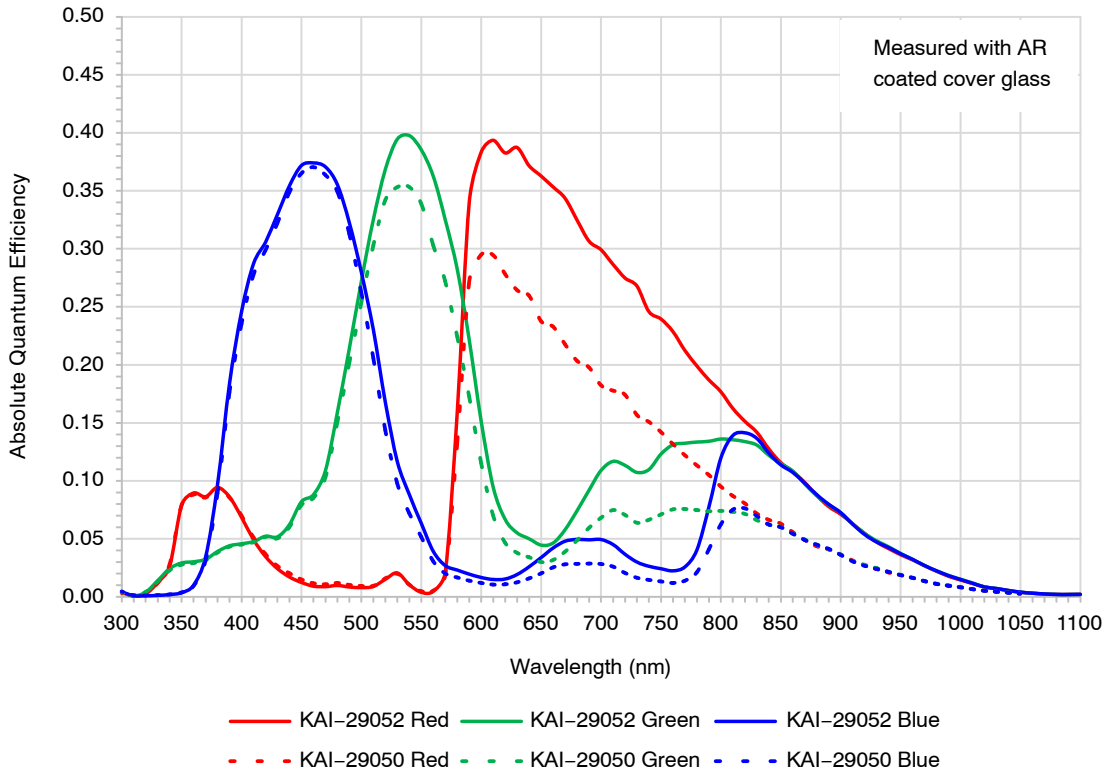


Figure 7. Color (Bayer RGB) with Microlens Quantum Efficiency

Color (Sparse FCA) with Microlens

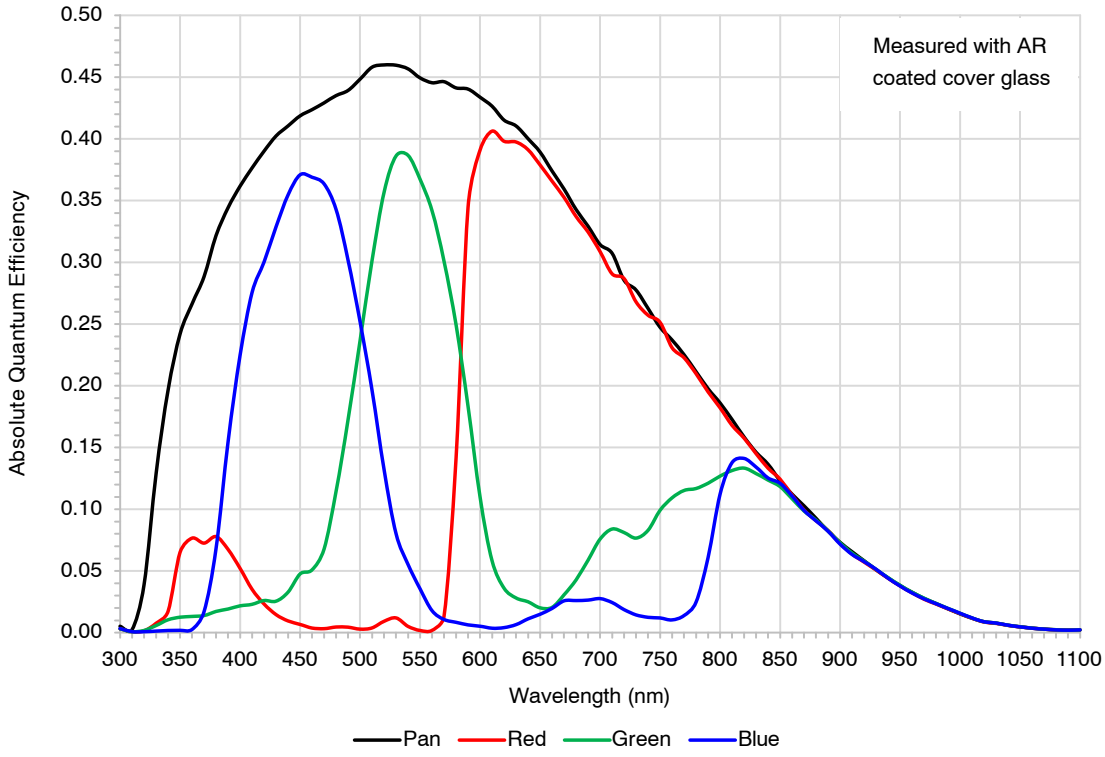


Figure 8. Color (Sparse CFA) with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

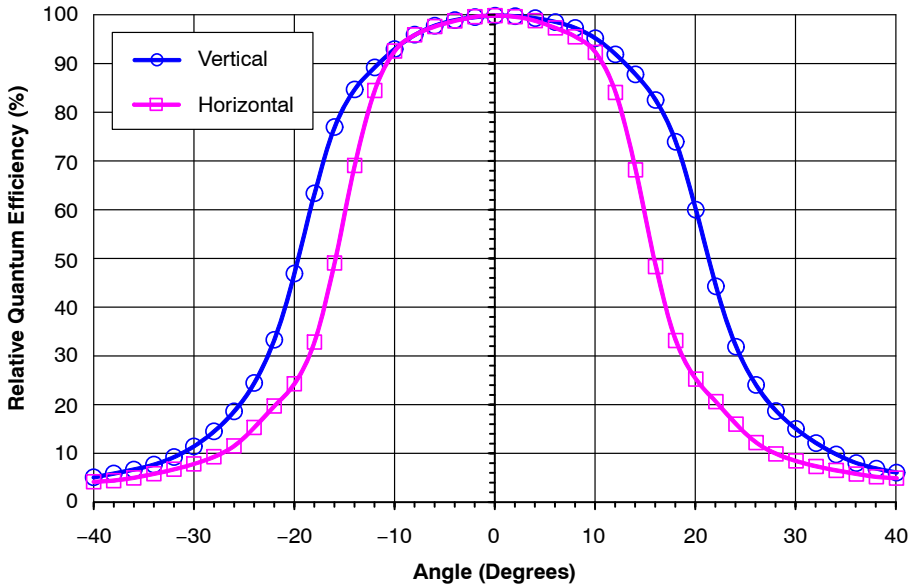


Figure 9. Monochrome with Microlens Angular Quantum Efficiency

Dark Current vs. Temperature

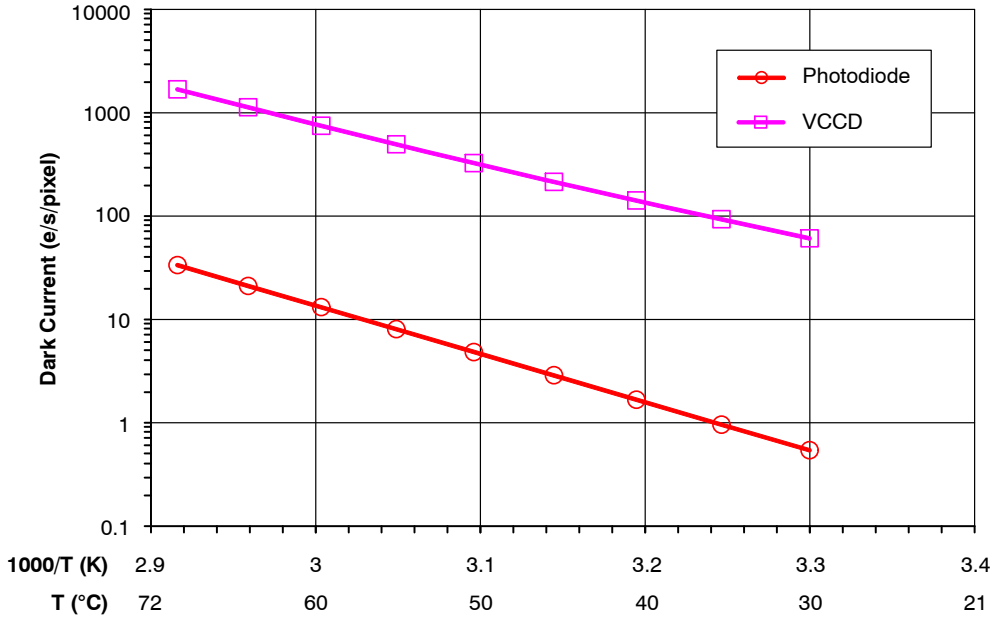


Figure 10. Dark Current vs. Temperature

Power − Estimated

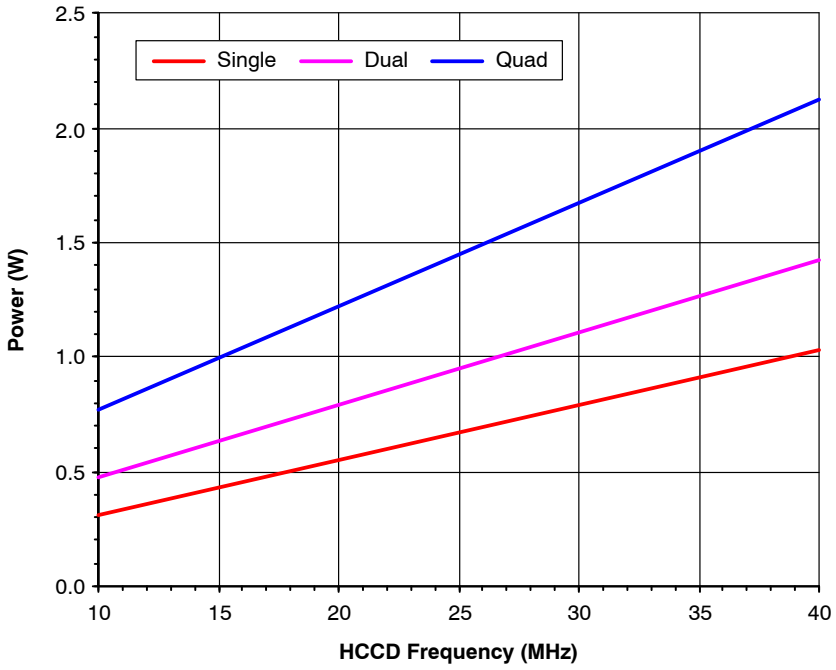


Figure 11. Power

Frame Rates

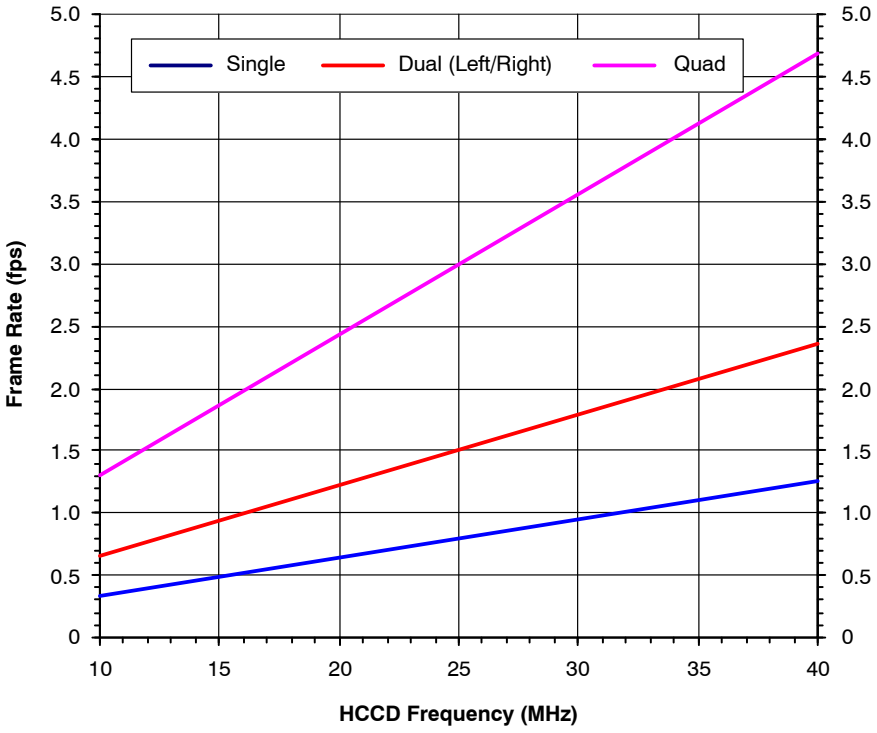


Figure 12. Frame Rates

DEFECT DEFINITIONS

Table 7. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

Description	Condition
Operational Mode	Two Outputs, using VOUTa and VOUTc, Continuous Readout
HCCD Clock Frequency	10 MHz
Pixels Per Line (Note 1)	6800
Lines Per Frame (Note 2)	2320
Line Time	715.7 μs
Frame Time	1660.5 ms
Photodiode Integration Time (PD_Tint)	Mode A: PD_Tint = Frame Time = 1660.5 ms, No Electronic Shutter Used
VCCD Integration Time (Note 3)	1593.1 ms
Temperature	40°C
Light Source (Note 4)	Continuous Red, Green and Blue LED Illumination
Operation	Nominal Operating Voltages and Timing

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 2226 lines × Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

Table 8. DEFECT DEFINITIONS FOR TESTING AT 40°C

Description	Definition	Grade 1	Grade 2 Mono	Grade 2 Color
Major Dark Field Defective Bright Pixel (Note 1)	PD_Tint = Mode A → Defect ≥ 565 mV	270	540	540
Major Bright Field Defective Dark Pixel (Note 1)	Defect ≥ 12%			
Minor Dark Field Defective Bright Pixel	PD_Tint = Mode A → Defect ≥ 282 mV	2700	5400	5400
Cluster Defect (Note 2)	A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally	20	N/A	N/A
Cluster Defect (Note 2)	A group of 2 to 38 contiguous major defective pixels, but no more than 5 adjacent defects horizontally	N/A	50	50
Column Defect (Note 2)	A group of more than 10 contiguous major defective pixels along a single column	0	7	27

1. For the color devices (KAI−29052−CXA and KAI−29052−QXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Table 9. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C

Description	Condition
Operational Mode	Two Outputs, using VOUTa and VOUTc, Continuous Readout
HCCD Clock Frequency	10 MHz
Pixels Per Line (Note 1)	6800
Lines Per Frame (Note 2)	2320
Line Time	715.7 μs
Frame Time	1660.5 ms
Photodiode Integration Time (PD_Tint)	Mode A: PD_Tint = Frame Time = 1660.5 ms, No Electronic Shutter Used
VCCD Integration Time (Note 3)	1593.1 ms
Temperature	27°C
Light Source (Note 4)	Continuous Red, Green and Blue LED Illumination
Operation	Nominal Operating Voltages and Timing

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 2226 lines × Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

Table 10. DEFECT DEFINITIONS FOR TESTING AT 27°C

Description	Definition	Grade 1	Grade 2 Mono	Grade 2 Color
Major Dark Field Defective Bright Pixel (Note 1)	PD_Tint = Mode A → Defect ≥ 565 mV	270	540	540
Major Bright Field Defective Dark Pixel (Note 1)	Defect ≥ 12%			
Cluster Defect (Note 2)	A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally	20	N/A	N/A
Cluster Defect (Note 2)	A group of 2 to 38 contiguous major defective pixels, but no more than 5 adjacent defects horizontally	N/A	50	50
Column Defect (Note 2)	A group of more than 10 contiguous major defective pixels along a single column	0	7	27

1. For the color devices (KAI−29052−CXA and KAI−29052−QXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 13: Regions of interest for the location of pixel 1, 1.

TEST DEFINITIONS

Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (6600, 4408)

Active Area ROI: Pixel (13, 13) to Pixel (6588, 4396)

Center ROI: Pixel (3251, 2155) to Pixel (3350, 2254)

Only the Active Area ROI pixels are used for performance and defect tests.

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 13 for a pictorial representation of the regions of interest.

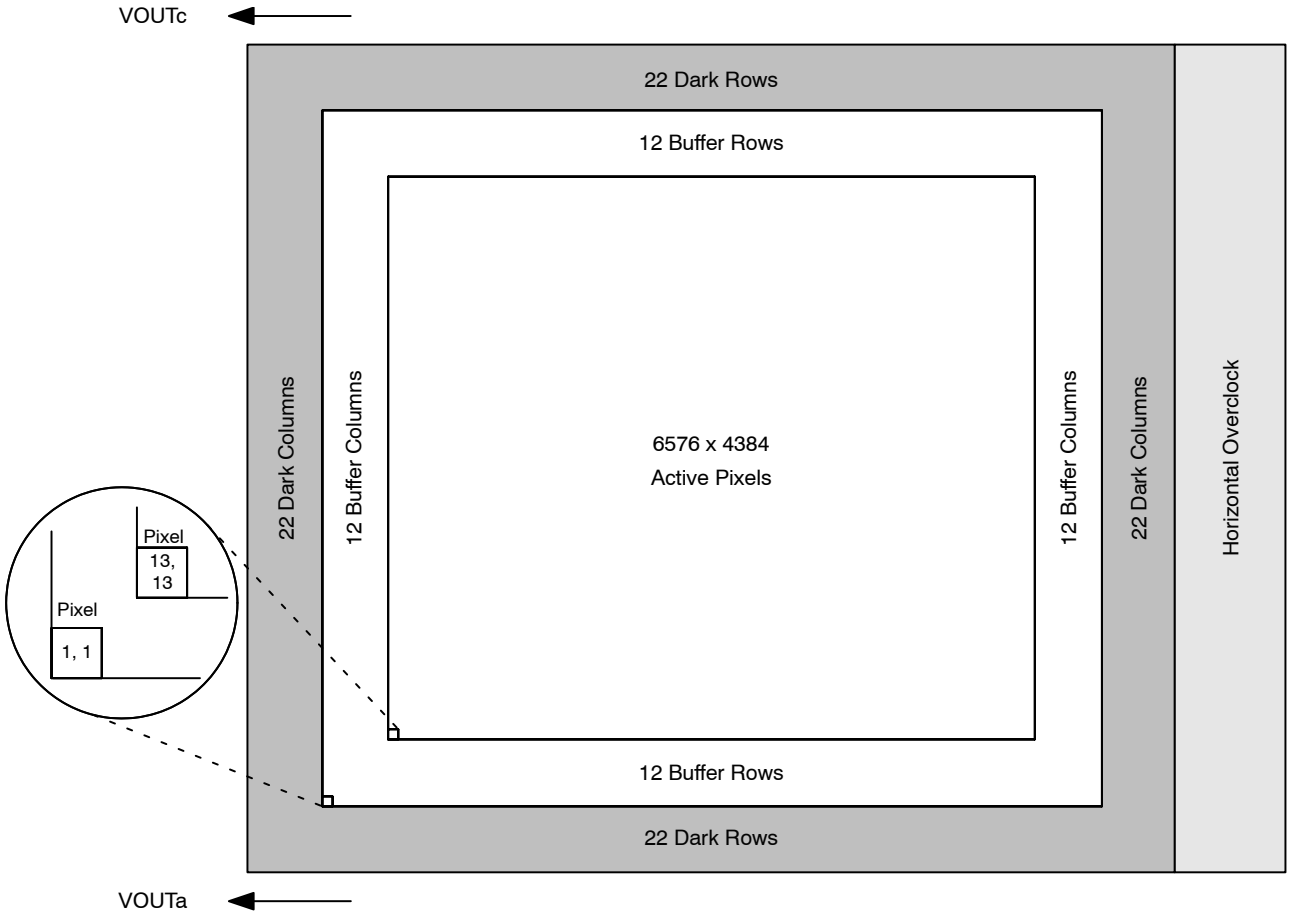


Figure 13. Regions of Interest

Tests

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. The average signal level of each of the 1536 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count} \ [\text{mV}] \quad \text{(eq. 1)}$$

Where i = 1 to 1536. During this calculation on the 1536 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

$$\text{Dark Field Global Non−Uniformity} = \text{Maximum Signal} - \text{Minimum Signal} \ [\text{mVpp}] \quad \text{(eq. 2)}$$

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 490 V). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 700 mV. Global non-uniformity is defined as:

$$\text{Global Non−Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}}\right) \ [\%\text{rms}] \quad \text{(eq. 3)}$$

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 490 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 700 mV. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. The average signal level of each of the 1536 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count} \ [\text{mV}] \quad \text{(eq. 4)}$$

Where i = 1 to 1536. During this calculation on the 1536 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Peak to Peak Non−Uniformity} = 100 \cdot \left(\frac{\text{Maximum Signal} - \text{Minimum Signal}}{\text{Active Area Signal}}\right) \ [\%\text{pp}] \quad \text{(eq. 5)}$$

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 490 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 700 mV. The average signal level of all active pixels is found. The dark threshold is set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold} \quad \text{(eq. 6)}$$

The sensor is then partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 490 mV
- Dark defect threshold: 490 mV · 12% = 59 mV
- Region of interest #1 selected. This region of interest is pixels 13, 13 to pixels 149, 149.
  - Median of this region of interest is found to be 495 mV.
  - Any pixel in this region of interest that is ≤ (495 – 59 mV) 436 mV in intensity will be marked defective.
- All remaining 1536 sub regions of interest are analyzed for defective pixels in the same manner.

OPERATION

Table 11. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit
Operating Temperature (Note 1)	T_{OP}	−50	70	°C
Humidity (Note 2)	RH	5	90	%
Output Bias Current (Note 3)	I_{OUT}	−	60	mA
Off-Chip Load	C_L	−	10	pF

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is −15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 12. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Unit
VDDα, VOUTα (Note 1)	−0.4	17.5	V
RDα (Note 1)	−0.4	15.5	V
V1B, V1T	ESD − 0.4	ESD + 24.0	V
V2B, V2T, V3B, V3T, V4B, V4T	ESD − 0.4	ESD + 14.0	V
FDGab, FDGcd	ESD − 0.4	ESD + 15.0	V
H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, Rα OGα (Note 1)	ESD − 0.4	ESD + 14.0	V
ESD	−10.0	0.0	V
SUB (Note 2)	−0.4	40.0	V

1. α denotes a, b, c or d.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions* − AND9183/D.

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

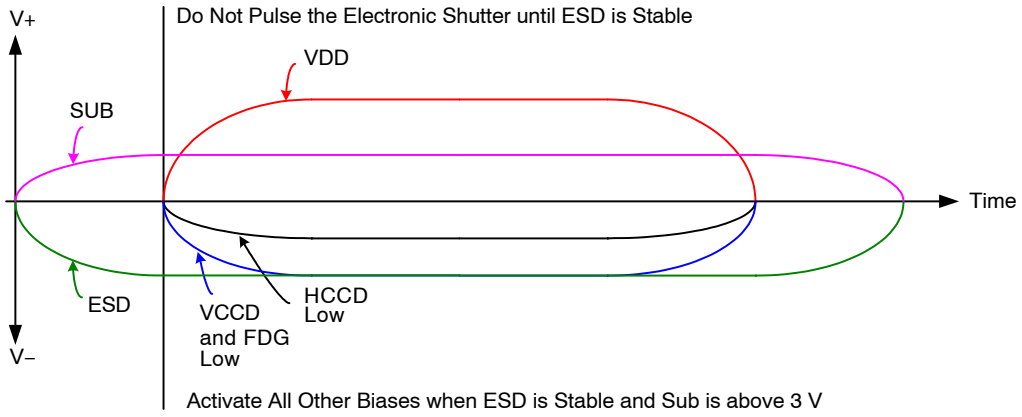


Figure 14. Power-Up and Power-Down Sequence

Warnings Regarding Power-Up and Power-Down

1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.
5. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD, and ESD during power-up and power-down. See figures shown below.

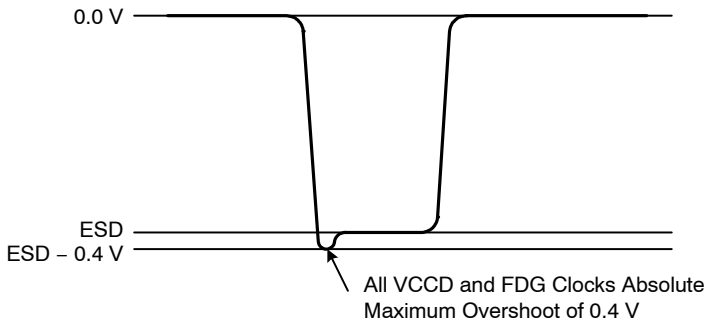


Figure 15. VCCD Overshoots

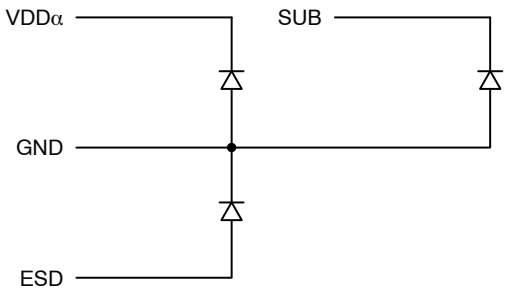


Figure 16. External Diode Protection

DC Bias Operating Conditions

Table 13. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Max. DC Current
Reset Drain (Note 1)	RDα	RD	11.8	12.0	12.2	V	10 μA
Output Gate (Note 1)	OGα	OG	−2.2	−2.0	−1.8	V	10 μA
Output Amplifier Supply (Notes 1, 2)	VDDα	V_{DD}	14.5	15.0	15.5	V	11.0 mA
Ground	GND	GND	0.0	0.0	0.0	V	−1.0 mA
Substrate (Notes 3, 8)	SUB	V_{SUB}	5.0	V_{AB}	V_{DD}	V	50 μA
ESD Protection Disable (Notes 6, 7)	ESD	ESD	−9.2	−9.0	−8.8	V	50 μA
Output Bias Current (Notes 1, 4, 5)	VOUTα	I_{OUT}	−3.0	−7.0	−10.0	mA	−

1. α denotes a, b, c or d.
2. The maximum DC current is for one output. $I_{DD} = I_{OUT} + I_{SS}$. See Figure 17.
3. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is the nominal P_{Ne} (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power-Up and Power-Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L + 0.4 V and V2_L + 0.4 V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions* − AND9183/D.

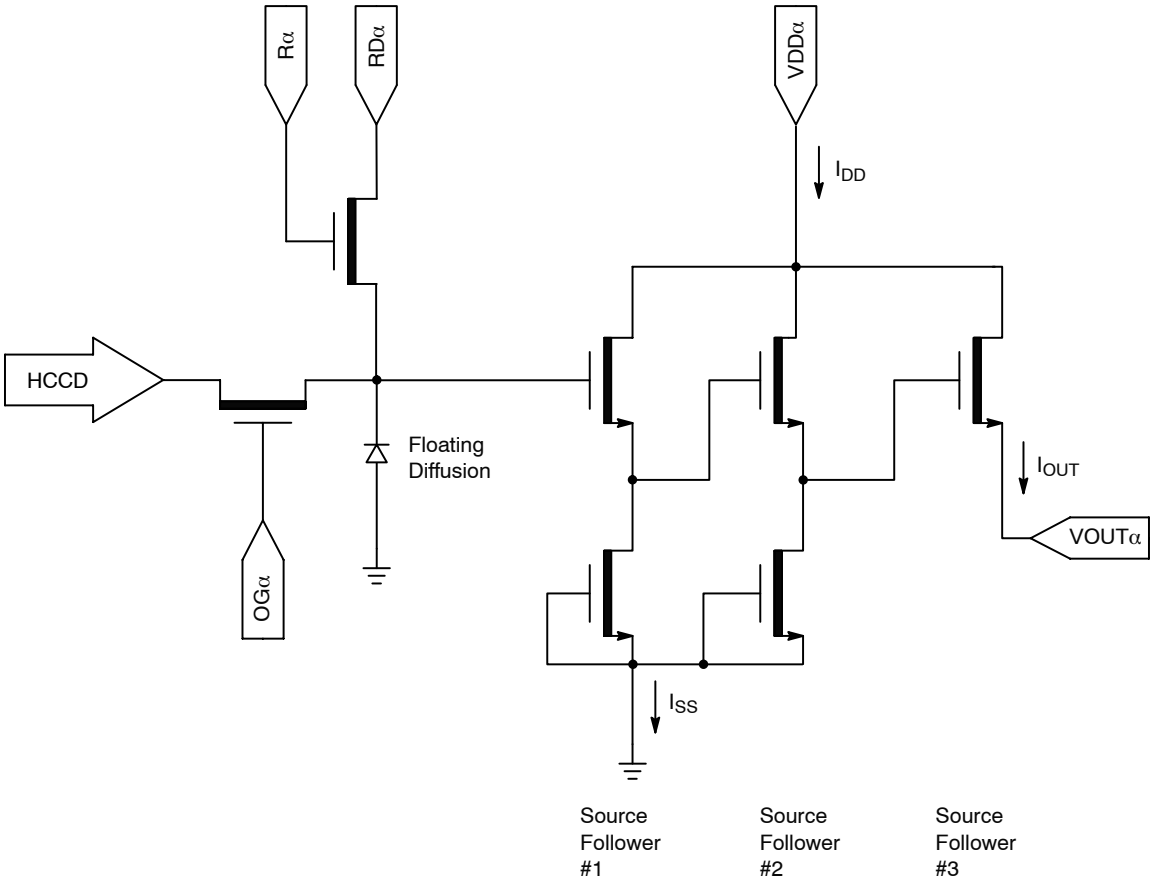


Figure 17. Output Amplifier

AC Operating Conditions

Table 14. CLOCK LEVELS

Description	Pins (Note 1)	Symbol	Level	Min.	Nom.	Max.	Unit	Capacitance (Note 2)
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	−9.2	−9.0	−8.8	V	180 nF (Note 6)
		V1_M	Mid	−0.2	0.0	0.2		
		V1_H	High	12.8	13.0	14.0		
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	−9.2	−9.0	−8.8	V	180 nF (Note 6)
		V2_H	High	−0.2	0.0	0.2		
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	−9.2	−9.0	−8.8	V	180 nF (Note 6)
		V3_H	High	−0.2	0.0	0.2		
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	−9.2	−9.0	−8.8	V	180 nF (Note 6)
		V4_H	High	−0.2	0.0	0.2		
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	−5.0 (Note 7)	−4.4	−4.2	V	600 pF (Note 6)
		H1S_A	Amplitude	4.2	4.4	5.0 (Note 7)		
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	−5.0 (Note 7)	−4.4	−4.2	V	400 pF (Note 6)
		H1B_A	Amplitude	4.2	4.4	5.0 (Note 7)		
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	−5.0 (Note 7)	−4.4	−4.2	V	580 pF (Note 6)
		H2S_A	Amplitude	4.2	4.4	5.0 (Note 7)		
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	−5.0 (Note 7)	−4.4	−4.2	V	400 pF (Note 6)
		H2B_A	Amplitude	4.2	4.4	5.0 (Note 7)		
Horizontal CCD Clock, Last Phase (Note 3)	H2SLα	H2SL_L	Low	−5.2	−5.0	−4.8	V	20 pF (Note 6)
		H2SL_A	Amplitude	4.8	5.0	5.2		
Reset Gate	Rα	R_L (Note 4)	Low	−3.5	−2.0	−1.5	V	16 pF (Note 6)
		R_H	High	2.5	3.0	4.0		
Electronic Shutter (Notes 5, 8)	SUB	VES	High	29.0	30.0	40.0	V	12 pF (Note 6)
Fast Line Dump Gate	FDGα	FDG_L	Low	−9.2	−9.0	−8.8	V	50 pF (Note 6)
		FDG_H	High	4.5	5.0	5.5		

1. α denotes a, b, c or d.
2. Capacitance is total for all like named pins.
3. Use separate clock driver for improved speed performance.
4. Reset low should be set to −3 volts for signal levels greater than 40,000 electrons.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions* − AND9183/D.
6. Capacitance values are estimated.
7. If the minimum horizontal clock low level is used (−5.0 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a −5.0 V to 0.0 V clock.
8. Figure 18 shown below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

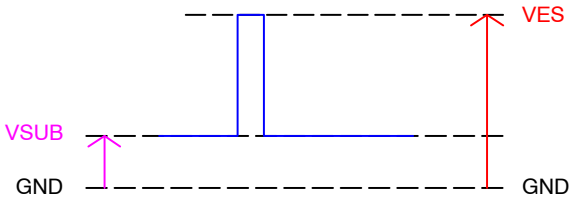


Figure 18. Substrate and Electron Shutter Reference to Ground

Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor 5.5 micron pixel interline CCD sensor is being used.

Table 15. DEVICE IDENTIFICATION

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Max. DC Current
Device Identification (Notes 1, 2)	DevID	DevID	200,000	300,000	400,000	Ω	50 μA

1. If the Device Identification is not used, it may be left disconnected.
2. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

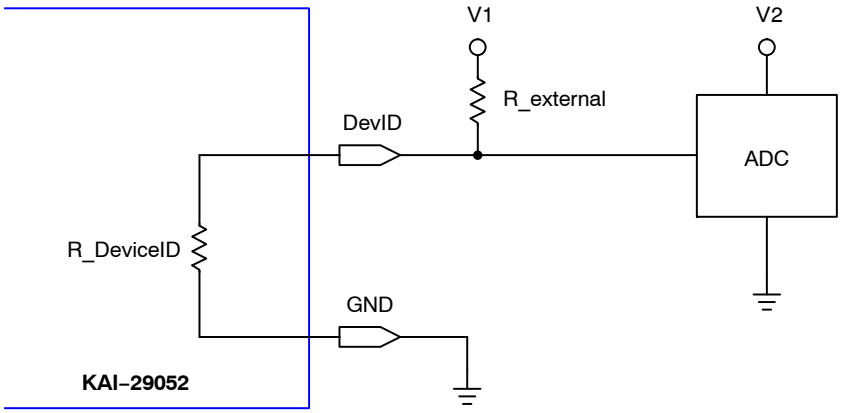


Figure 19. Device Identification Recommended Circuit

TIMING

Table 16. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Photodiode Transfer	t_{PD}	6	–	–	μs	
VCCD Leading Pedestal	t_{3P}	16	–	–	μs	
VCCD Trailing Pedestal	t_{3D}	16	–	–	μs	
VCCD Transfer Delay	t_D	4	–	–	μs	
VCCD Transfer	t_V	8	–	–	μs	
VCCD Clock Cross-Over	V_{VCR}	75	–	100	%	1
VCCD Rise, Fall Times	t_{VR}, t_{VF}	5	–	10	%	1, 2
FDG Delay	t_{FDG}	2	–	–	μs	
HCCD Delay	t_{HS}	1	–	–	μs	
HCCD Transfer	t_e	25.0	29.4	–	ns	
Shutter Transfer	t_{SUB}	1	–	–	μs	
Shutter Delay	t_{HD}	1	–	–	μs	
Reset Pulse	t_R	2.5	–	–	ns	
Reset − Video Delay	t_{RV}	–	2.2	–	ns	
H2SL − Video Delay	t_{HV}	–	3.1	–	ns	
Line Time	t_{LINE}	96.3	110.0	–	μs	Dual HCCD Readout
		179.4	208.7	–		Single HCCD Readout
Frame Time	t_{FRAME}	213.5	246.1	–	ms	Quad HCCD Readout
		427.0	492.2	–		Dual HCCD Readout
		795.1	925.2	–		Single HCCD Readout

1. Refer to Figure 24: VCCD Clock Rise Time, Fall Time, and Edge Alignment.
2. Relative to the pulse width.

Timing Diagrams

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1−P7) as shown in the table below. The patterns are defined in Figure 20 and Figure 21. Contact ON Semiconductor Application Engineering for other readout modes.

Table 17. TIMING DIAGRAMS

Device Pin	Quad Readout	Dual Readout VOUTa, VOUTb	Dual Readout VOUTa, VOUTc	Single Readout VOUTa
V1T	P1T	P1B	P1T	P1B
V2T	P2T	P4B	P2T	P4B
V3T	P3T	P3B	P3T	P3B
V4T	P4T	P2B	P4T	P2B
V1B	P1B			
V2B	P2B			
V3B	P3B			
V4B	P4B			
H1Sa	P5			
H1Ba				
H2Sa (Note 2)	P6			
H2Ba				
Ra	P7			
H1Sb	P5		P5	
H1Bb			P6	
H2Sb (Note 2)	P6		P6	
H2Bb			P5	
Rb	P7		P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)
H1Sc	P5	P5 (Note 1) or Off (Note 3)	P5	P5 (Note 1) or Off (Note 3)
H1Bc				
H2Sc (Note 2)	P6	P6 (Note 1) or Off (Note 3)	P6	P6 (Note 1) or Off (Note 3)
H2Bc				
Rc	P7	P7 (Note 1) or Off (Note 3)	P7	P7 (Note 1) or Off (Note 3)
H1Sd	P5	P5 (Note 1) or Off (Note 3)	P5	P5 (Note 1) or Off (Note 3)
H1Bd			P6	
H2Sd (Note 2)	P6	P6 (Note 1) or Off (Note 3)	P6	P6 (Note 1) or Off (Note 3)
H2Bd			P5	
Rd	P7	P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)

#Lines/Frame (Minimum)	2226	4452	2226	4452
#Pixels/Line (Minimum)	3333		6666	

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx. For optimal speed performance, use a separate clock driver.
3. Off = +5 V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 2226 or 4452 minimum counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1−P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid-state when P4 transitions from the low state to the high state.

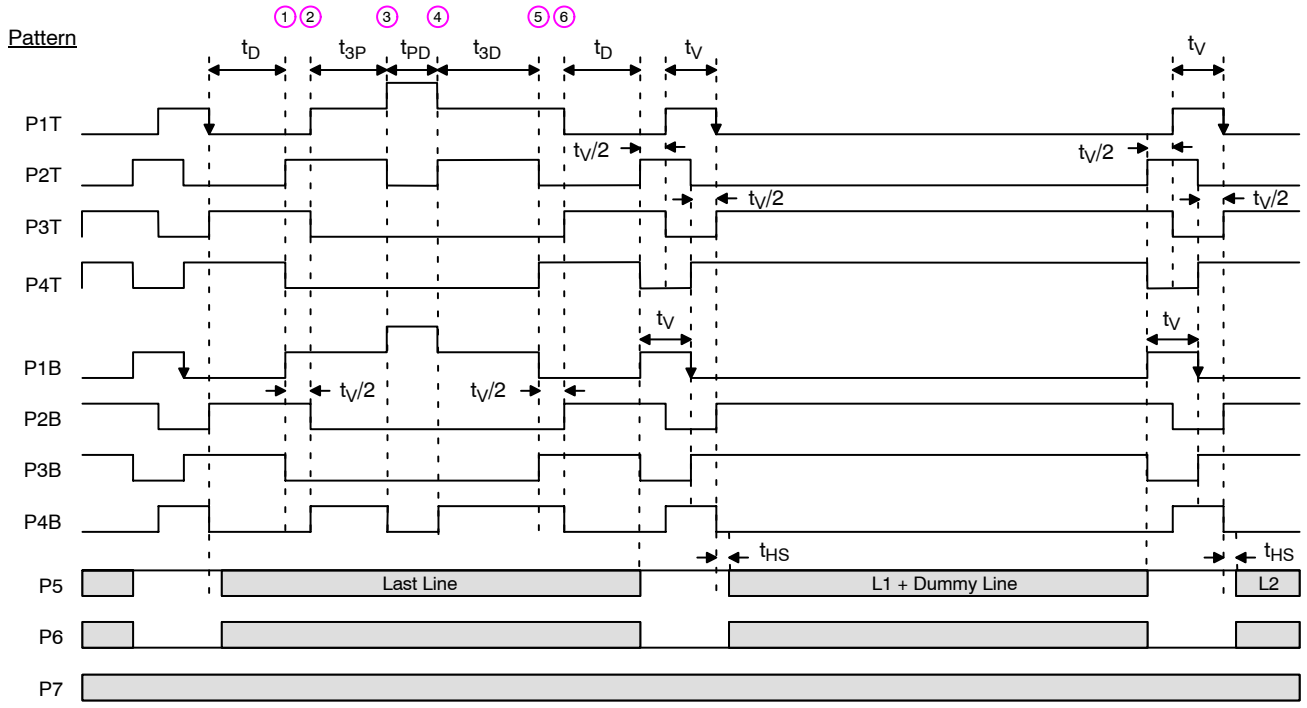


Figure 20. Photodiode Transfer Timing

Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependent on readout mode – either 3333 or 6666 minimum counts required.

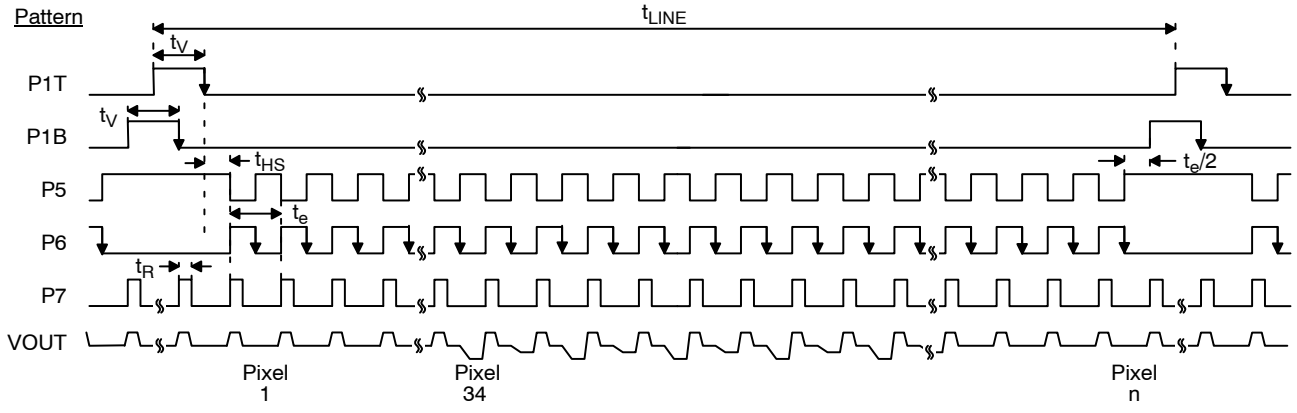


Figure 21. Line and Pixel Timing

Pixel Timing Detail

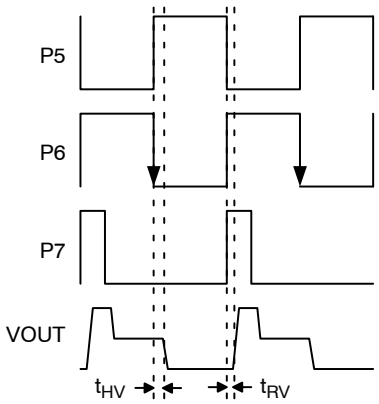


Figure 22. Pixel Timing Detail

Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below. The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

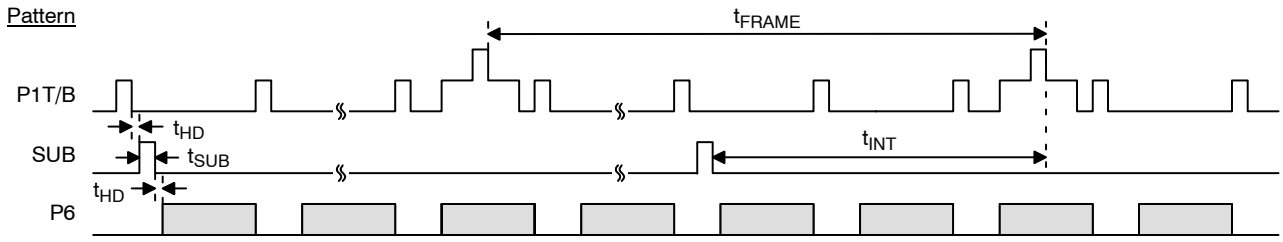


Figure 23. Electronic Shutter Timing

VCCD Clock Edge Alignment

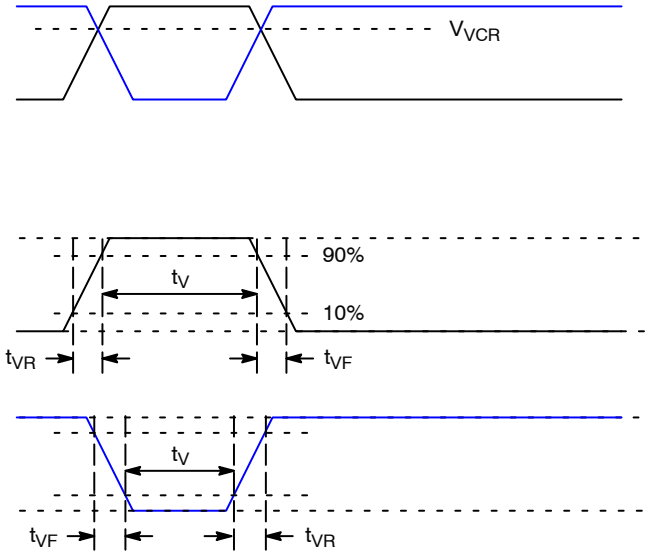


Figure 24. VCCD Clock Rise Time, Fall Time, and Edge Alignment

Line and Pixel Timing − Vertical Binning by 2

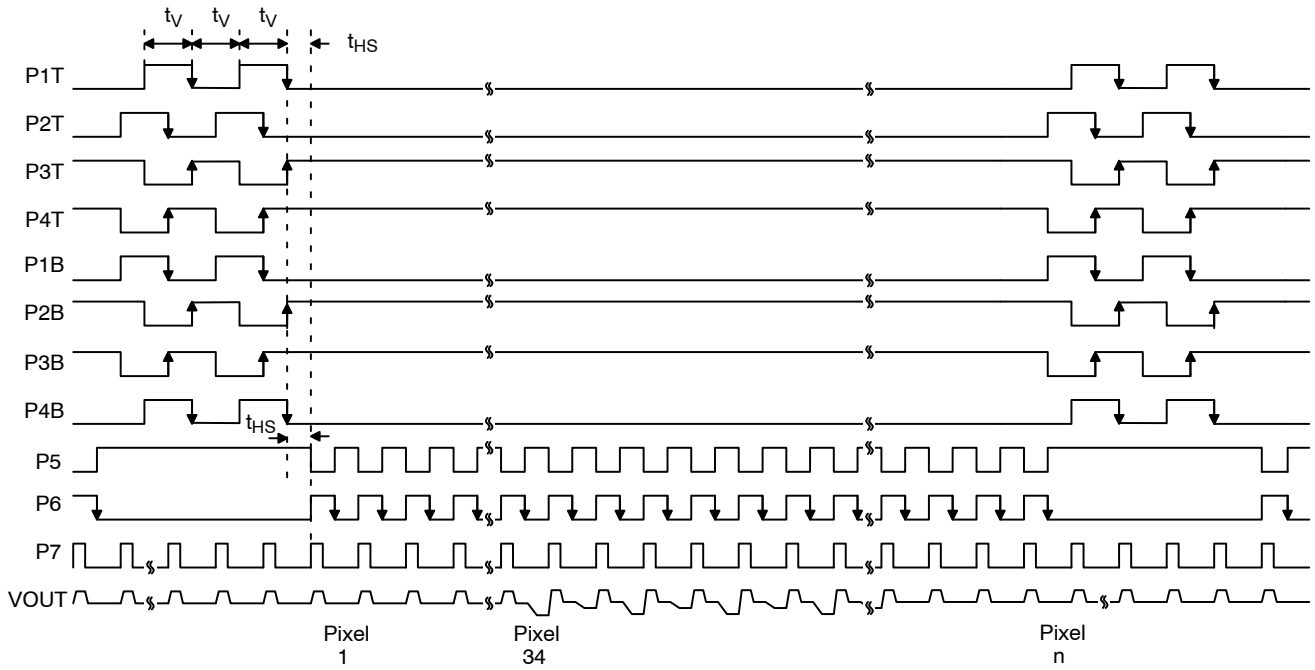


Figure 25. Line and Pixel Timing − Vertical Binning by 2

Fast Line Dump Timing

The FDG pins may be optionally clocked to efficiently remove unwanted lines in the image resulting for increased frame rates at the expense of resolution. Below is an example of a 2 line dump sequence followed by a normal readout line.

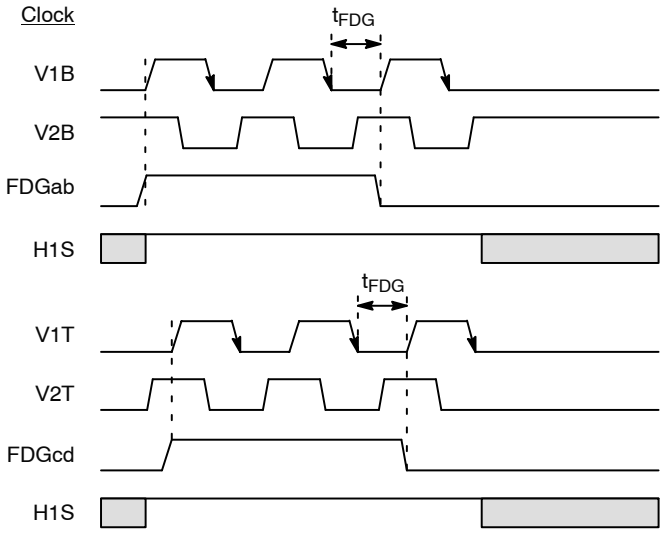


Figure 26. Fast Line Dump Timing

STORAGE AND HANDLING

Table 18. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit
Storage Temperature (Note 1)	T_{ST}	−55	80	°C
Humidity (Note 2)	RH	5	90	%

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

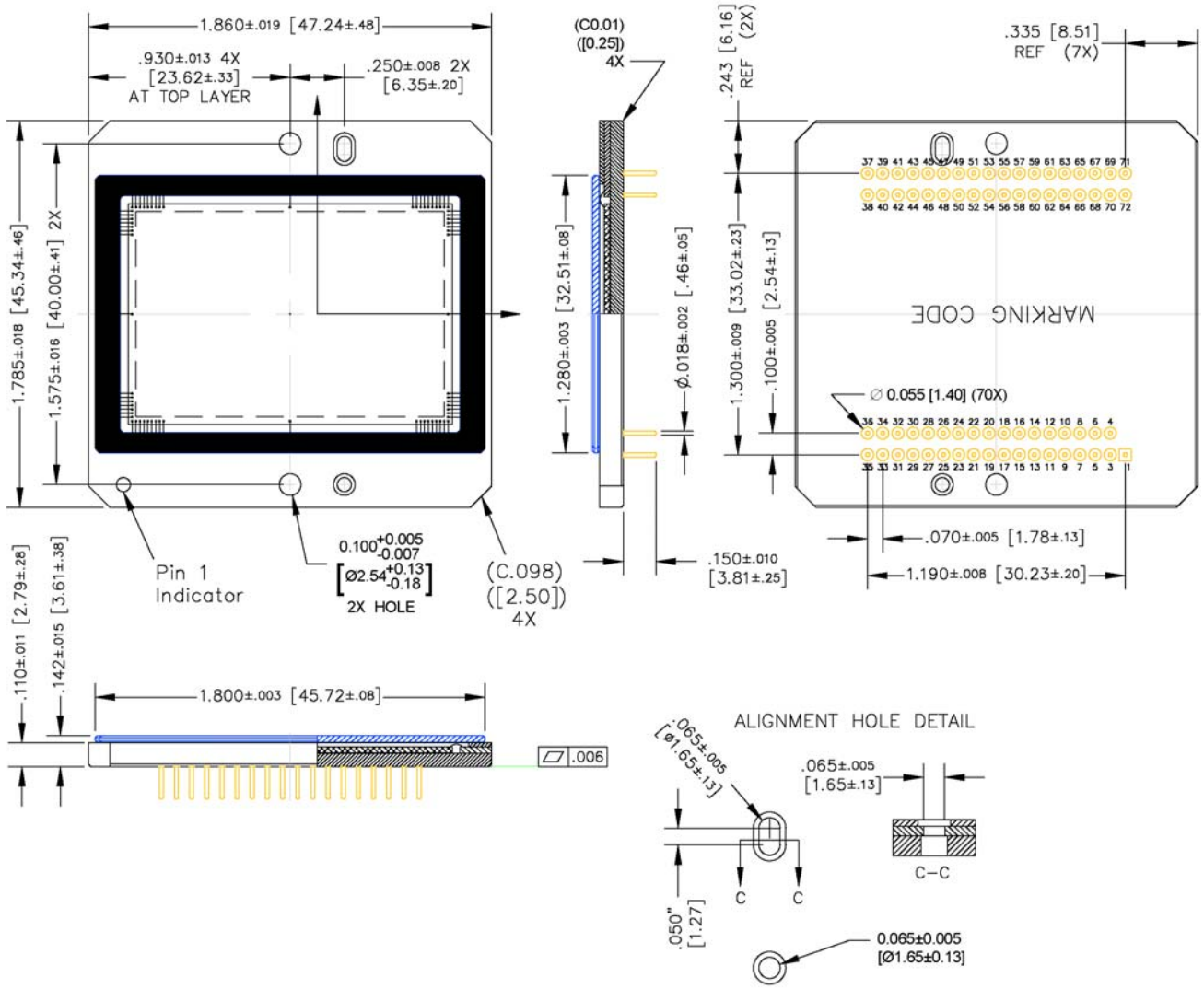
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

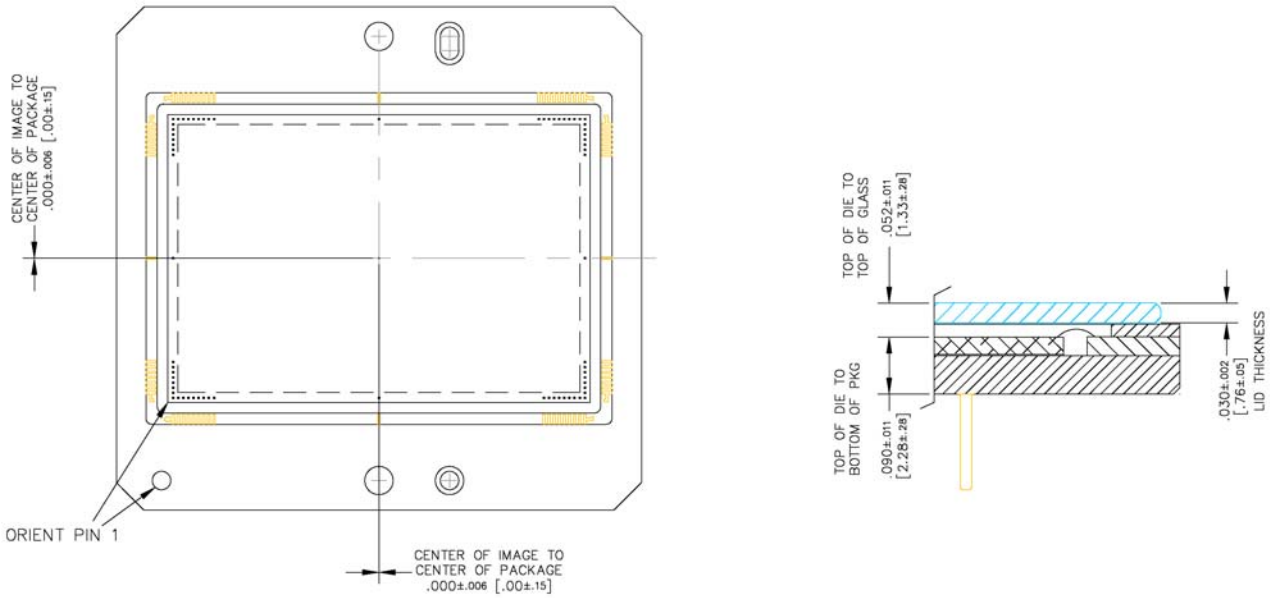
MECHANICAL INFORMATION

Completed Assembly



Notes:
1. See Ordering Information for marking code.
2. Cover glass not to overhang package holes or outer ceramic edges.
3. Glass epoxy not to extend over image array.
4. No materials to interfere with clearance through package holes.
5. Units: IN [MM].

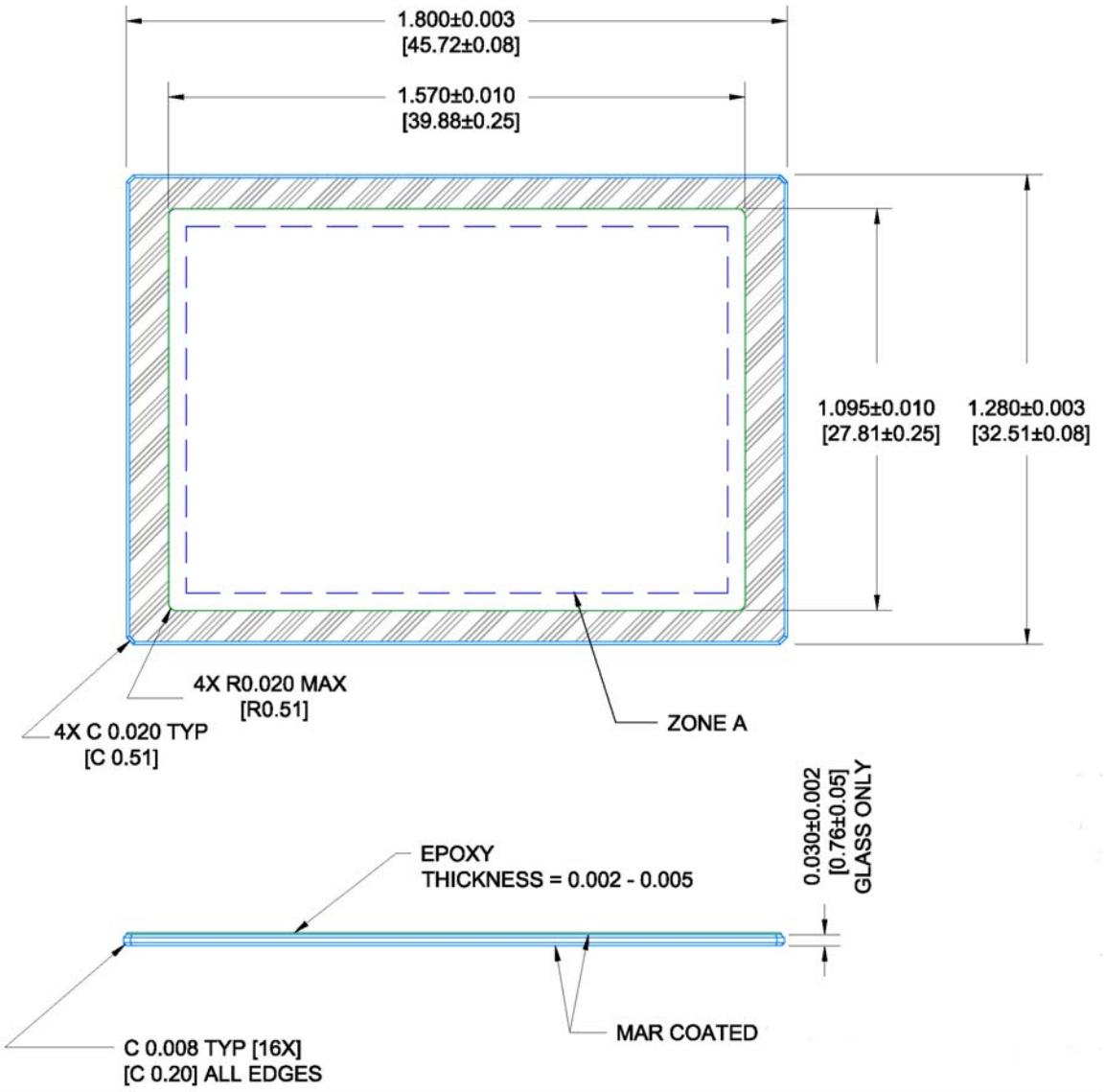
Figure 27. Completed Assembly (1 of 2)



Notes:
1. Units: IN [MM].

Figure 28. Completed Assembly (2 of 2)

Cover Glass



Notes:
1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
   a. 20_m Max size in Zone A
   b. Zone A = 1.474 × 1.000 [16.43 × 10.08] Centered
3. MAR coated both sides
4. Spectral Transmission
   a. 350−365 nm: T ≥ 88%
   b. 365−405 nm: T ≥ 94%
   c. 405−450 nm: T ≥ 98%
   d. 450−650 nm: T ≥ 99%
   e. 650−690 nm: T ≥ 98%
   f. 690−770 nm: T ≥ 94%
   g. 770−870 nm: T ≥ 88%
5. Units: IN [MM]

Figure 29. Cover Glass

Cover Glass Transmission

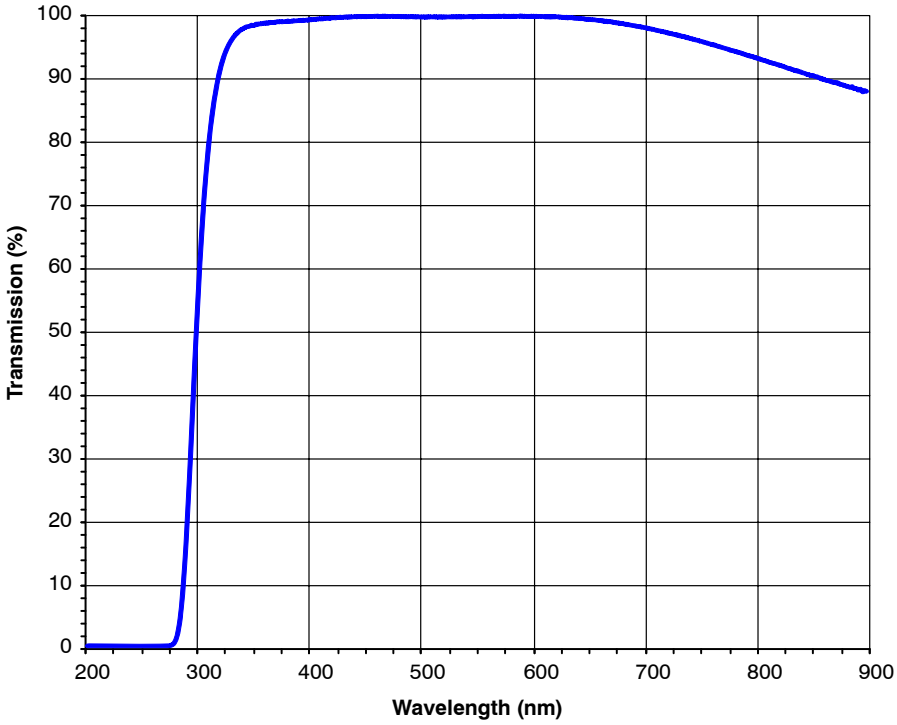


Figure 30. Cover Glass Transmission

PUBLICATION ORDERING INFORMATION

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19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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